REMARKS

Claims 1-38 were pending in the application. Claims 28-36 were previously withdrawn from consideration. By way of the present amendment, claims 1, 14, 26 and 28-38 are being canceled, leaving claims 2-13, 15-25, and 27 pending.

In a proposed drawing change being submitted herewith, Fig. 1 is being labeled as prior art. The informalities noted in the Office action on page 4, line 7 and on page 11, line 20 have been corrected. Accordingly, it is respectfully requested that the objection to the specification be withdrawn.

Claims 1-27, 37, and 38 stand rejected as described below.

Claims 1-5, 10, 17, 22, and 23 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Devanney (U.S. Pat. No. 6,191,641). That rejection is respectfully traversed with respect to amended claim 2, for the following reasons. Claim 2 now incorporates the subject matter of claims 1, 2, and 14 and thus corresponds to claim 14 as originally submitted. Claim 14 was not rejected as anticipated by Devanney and thus amended claim 2 is believed to distinguish for that reason. In addition, amended claim 2 recites, in part, a package mounting at least one integrated circuit die and that the first end of the one-time programmable element is coupled to a power supply voltage in the package. Devanney fails to teach a one-time programmable element in a package for mounting an integrated circuit die.

Claim 17 has been amended to incorporate the subject matter of claim 26 and recites in part a package including one or more one-time programmable elements. Claim 26 was not rejected as anticipated by Devanney and thus amended claim 17 is believed to distinguish for that reason. In addition, Devanney fails to teach anything about a package with one-time programmable elements. Accordingly, since Devanney fails to teach elements specifically recited in independent claim 17, the Applicants respectfully submit that amended claim 17 distinguishes over Devanney. Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) be reconsidered and withdrawn as to claims 2 and 17, and all claims dependent thereon.

Claims 1-5, 7, 8, 11, 20, 22, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hilgers (U.S. Pat. No. 4,626,818). That rejection is respectfully traversed with respect to amended claim 2, for the following reasons. Hilgers discloses a fusable device for use in preventing thick film networks. As claim 2 now incorporates the subject matter of claims 1, 2 and 14 and claim 14 was not rejected as anticipated by Hilgers, amended claim 2 is believed to distinguish for that reason. In addition, Hilgers fails to teach a package that comprises a one-time programmable element having an end coupled to a power supply voltage node in the package as recited in amended claim 2. Accordingly, Applicants respectfully request that the rejection of claim 2 and all claims dependent thereon be reconsidered and withdrawn.

The Office action failed to reject independent claim 17 as being anticipated by Hilgers. Accordingly, claims 20, 22, and 23 cannot be anticipated if claim 17 is not anticipated. Accordingly, Applicants respectfully request that the rejection of claim 20, 22, and 23 be reconsidered and withdrawn.

Claims 1-3, 7, 9, 17, 18, 37, and 38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bohr (U.S. Pat. No. 5,708,291). As claim 2 now incorporates the subject matter of claims 1, 2 and 14 and claim 14 was not rejected as anticipated by Bohrs, amended claim 2 is believed to distinguish for that reason. In addition, Bohr teaches at col. 1, lines 11-13 that the Bohr invention relates particularly to fusable link devices in semiconductor integrated circuits. Bohr fails to teach programmable elements on a package as required by amended claims 2 and 17. In addition, as amended claim 17 now incorporates the subject matter of claim 26 and claim 26 was not rejected as anticipated by Bohrs, amended claim 17 is believed to distinguish for that reason.

Accordingly, Applicants respectfully request that the rejection of claims 2 and 17 and all claims dependent thereon be reconsidered and withdrawn.

The cancellation of claim 37 and 38 render their rejection moot.

Claims 1, 2, 7-9, 11, 12, 14-18, 20-23, 26, and 27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Crafts (U.S. Pat. No. 5,536,968). Crafts teaches a programmable read only memory (PROM) including an array of polysilicon fuse elements. See Abstract. Crafts

fails to teach anything about one-time programmable elements being located on a package for a semiconductor device as required by amended independent claim 2, 12, 17, and 21. Accordingly, Applicants respectfully submit that the independent claims distinguish over Crafts and respectfully request that the rejection of those claims and all claims dependent thereon be reconsidered and withdrawn.

Claims 1-4, 7, 9, 10-13, 17, 18, 20, 21, 26, 37, and 38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nathan (U.S. Pat. No. 5,813,881). The Office action points to Fig. 1 of Nathan as showing the fuse structures claimed in the above-identified claims. However, Applicants note that Fig. 1 illustrates a matrix of fuses manufactured on a printed circuit board in accordance with one embodiment of the invention. See col. 5, lines 59-61. Thus, Applicants respectfully maintain that the portion of Nathan cited by the Examiner fails to teach the package for mounting at least one integrated circuit die that comprises at least one-time programmable element having an end coupled to a power supply voltage node in the package as recited in amended claim 2.

Further, amended claim 2 now recites a pair of programmable elements. Specifically, amended claim 2 now recites that the package includes at least one pair of programmable elements, the one pair including the one one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first -one-time programmable element.

The structure claimed by amended claim 2 (subject matter originally in claim 14) is illustrated in Figs. 6-10 of the application, where pairs of programmable elements, e.g., elements 601 and 602 are shown. Note that in the embodiment illustrated in Figs. 6-10, at least one fuse of each pair must be blown to connect the common node to either of the supply voltages Vcc or Vss. Note that if three state logic is available, then both fuses of the pair can be cut to represent a third value. Applicants respectfully submits that the structure in amended claim 2 and illustrated in Figs. 6-10 is not shown in Nathan, alone or in combination with other references of

record. Accordingly, Applicants respectfully submit that claim 14 is patentable over the art of record.

Claim 12 has been amended to incorporate the subject matter of claim 1 and is now in independent form. Claim 12 recites that another programmable element is coupled between the second end of the programmable element and an external package connection. That structure is shown, for example, in Fig. 8 where programmable elements 624-627 are coupled between the second end of programmable element 601-607 and external package connectors. The structure illustrated in Fig. 8 provides, as described on page 10, lines 3-7 of the application, that the fuses 624-627 can be used in testing environments, where, for example, an internal signal must be accessible during test, but is then decoupled from the package pin by blowing a fuse prior to product shipment. That claimed structure and the advantage referenced above is not taught or suggested in any of the references of record alone or in combination. Accordingly, Applicants respectfully submit that claim 12 is patentable over the art of reference.

Claim 21 has been amended to include the subject matter of claim 17 and is now independent. Claim 21 is believed to be patentable for the same reasons as described in relation to claim 12.

Claim 13 has been put in independent form by incorporating the subject matter of claim 1. Claim 13 recites that a second one-time programmable element is coupled in parallel with the one one-time programmable element of claim 1 and that the one one-time programmable element is a fuse and the second one-time programmable element is an antifuse. That claimed structure is shown in Fig. 13 of the application. That structure, as described on page 11, lines 24-25, provides capability to reverse a fuse cut. That structure is not taught or suggested in the references of record. Accordingly, Applicants respectfully submit that claim 13 is patentable for that reason.

Claims 19, 24, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Crafts (U.S. Pat. No. 5,536,968) and further in view of Barth (U.S. Pat. No. 5,134,616). As applicants have explained Crafts fails to teach the a package including one or more one-time programmable elements as recited in claim 17 on which claims 19 and 24 depend. That teaching

is not supplied in Barth. Accordingly, applicants respectfully request that the rejection of claim 19 and 24 be reconsidered and withdrawn.

Claim 25 has been amended to be in independent form and incorporates the subject matter of claim 17. The Office action rejects claim 25 relying on Barth, col. 12, lines 10-34 to teach a semiconductor memory device wherein fuses are programmed to perform an error correction. However, that fails to teach that the programmable element specifies use of ECC for the cache memory on the integrated circuit as claimed in claim 25. Instead Barth teaches using fuses to achieve redundancy by efficiently switching in redundant bit lines. See Summary of the Invention. Barth fails to teach or suggest specifying use of ECC using a programmable element as claimed in claim 25. Accordingly, Applicants respectfully submit that claim 25 distinguishes over the references of record.

Claim 6 stands rejected under 35 U.S.C. § 103(a) s being unpatentable over Devanney. The Office action maintains that it would have been obvious to one of skill in the art to have excluded the protective layer recited in claim 6. However, Applicants respectfully submit that Devanney fails to teach a package as recited in amended claim 2. Accordingly, Applicants respectfully submit that the Office action fails to establish a prima facia case of obviousness of claim 6 over Devanney for at least that reason.

In view of the above amendments and remarks, applicants believe that all claims are now in condition for allowance. However, if the Examiner believes there are any issues which could be resolved via a telephone conference, the Examiner is respectfully requested to contact the undersigned at the number indicated below.

MARKED-UP COPY OF REPLACED PARAGRAPHS OF SPECIFICATION IN ACCORDANCE WITH 37 C.F.R. § 121(b)(iii)

Please amend the paragraph beginning on page 4, line 4 as follows:

Still another embodiment provides a method for setting a parameter value for an integrated circuit. The method includes selectively programming one or more programmable elements located on an integrated circuit package, to selectively couple an internal package node to a supply voltage node. The one or more programmable elements are selectively programmed according to a desired value of an integrated circuit parameter. The parameter may, e.g., be a voltage or speed rating. The internal package node is coupled to either a package pin, an input terminal of the integrated circuit or both.

Please amend the paragraph beginning on page 11, line 17 as follows:

In one embodiment, an antifuse such as the one illustrated in Fig. 12 may be utilized. The antifuse 120 includes a generally circular conductive area 121 which is in electrical contact with via 122. Via 122 may couple, e.g., to a power supply node. Via 123 is not in electrical contact with via [123] 122. If it is desired to short via 122 and 123 together, then conductive paste or solder may be deposited so as to form an electrical contact between via 123 and via 122 and circular conductive area 121. The conductive paste may then be subject to ultraviolet curing.

MARKED-UP COPY OF AMENDED CLAIMS IN ACCORDANCE WITH 37 C.F.R. § 121(c)(ii)

1. Canceled.

2 7. (Amended) A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package [The package as recited in claim 1] and wherein the programmable element is one of a fuse and an antifuse; and wherein

the package includes at least one pair of programmable elements, the one pair including the one one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first -one-time programmable element.

12. (Amended) A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package and wherein the [The] package [as recited in claim 2] further [comprising] comprises another programmable element coupled between the second end of the programmable element and an external package connection.

13. (Amended) A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package [The package as recited in claim 1

further comprising] and wherein a second one-time programmable element is coupled in parallel with the one time programmable element and wherein the one one-time programmable element is a fuse and the second one-time programmable element is an antifuse.

14. Canceled.

15. (Amended) The package as recited in claim [14] 2 wherein the internal package node is coupled to at least one of an external package connection and an input terminal of the integrated circuit die, after mounting of the integrated circuit die.

16. (Amended) The package as recited in claim [14] 2 further comprising a first resistive element coupled between the internal package node and the power supply node and a second resistive element coupled between the internal package node and the second power supply node.

17. (Amended) An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node; [and]

at least one integrated circuit die mounted in the package; and

wherein the one one-time programmable element is part of a one-time programmable element pair, the programmable element pair including a second one-time programmable element in addition to the one one-time programmable element, the second programmable element having a first end coupled to the internal package node and a second end coupled to a second power supply voltage.

21. (Amended) An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the

package and a second end of the programmable link is coupled to an internal package node;

at least one integrated circuit die mounted in the package; and

[The electronic device as recited in claim 20] wherein the internal package node couples to an external package connection through another one-time programmable element.

25. (Amended) An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node; and

at least one integrated circuit die mounted in the package and [The electronic device as recited in claim 17] wherein a state of the programmable element specifies use of error correction code (ECC) for a cache memory on the [processor] integrated circuit.

26. Canceled.

27. (Amended) The electronic device as recited in claim [26] 17 further comprising a first resistive element coupled respectively between the internal package node and the first power supply node and a second resistive element coupled between the internal package node and the second power supply node, thereby providing a voltage divider when the first power supply node is electrically coupled to the second power supply node through the programmable element pair.

28. - 38. Canceled.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on the date shown below.

Mark Zagorin — 3/19/2002
Mark Zagorin — Date

Respectfully submitted,

Mark Zagorin, Reg. No. 36,067
Attorney for Applicant(s)
(512) 347-9030
(512) 347-9031 (fax)